Name of the Teacher: Shilpa Gogia Class: BSc Electronics 3rd sem(paper2)

**Lesson Plan**

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| **S No** | **Period** | **Topics to be Covered** | **Academic Activity to be Organized** |
|  | **17-31 July 2017** | **UNIT -1 Combinational Circuit – I**  Half adder, full adder, half subtractor, full subtractor, parallel binary adder, 8421 adder., 2’S complement adder/ subtractor, Digatal Comparator | **Oral discussion** |
|  | **01-31 Aug 2017** | **UNIT -2 Combinational Circuit – II**  Multiplexers and their use in combinational logic circuit design, Demultiplexer, Decoder and their use in combinational logic circuit design, Parity generator and checker, code converter, BCD to Seven Segment, BCD to Cyclic Code, Binary to Decimal, Binary to Gray, Binary to Excess-3. | **Board test** |
|  | **01-30 Sept 2017** | **UNIT -3 Sequential Circuits I**  Basic sequential circuit, Asynchronous and Synchronous circuits, flip- flops, R-S and J-K flip, Master Slave flip flop, J-K flip flop | **Presentations** |
|  | **01-31 Oct 2017** | T and D flip flop, Analysis of Clocked sequential Circuits.  **UNIT -IV - Sequential Circuits II**  Counters: Asynchronous counters- Mod-N or divided by N Counter,Synchronous counter - Modulo Counters, Decade counter. | **Group Discussion** |
|  | **01-13 Nov 2017** | UP-Down counters, Basic principles of digital clock | **Problems & Solutions** |

**Topics of Assignments/ Class Tests to be given to the Students:**

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| Assignment 1 | Q1 Design binary to Excess-3 coide convertor.  Q2 Differentiate between as Asynchronous and synchronous circuit.  Q3 Differentiate between decoder and demultiplexer.  Q4 Design a full adder using two half adders. |
| Assignment 2 | Q1 What is race in Asynchronous circuit?  Q2 Explain clocked SR F-F.  Q3 What is the problem with SR F-F? Explain JK F-F. |
| Class Test | Q1 Design a 3 bit even parity generator.  Q2 Implement the following functions using a suitable decoder  F1(A,B,C)=ΣM(0,2,3,4,7) F2(A,B,C)=Σ(0,2,4,6).  Q3 How will you design a 16:1 MUX using 4:1 MUX. |