**Name of the Teacher:** Magandeep Kaur **Class:** B.Sc (Hons)-IT-I-SEM-I

**Subject:** Digital Electronics-I  **Paper:** BSIT-104

**Lesson Plan**

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| **S No** | **Period** | **Topics to be Covered** | **Academic Activity to be Organized** |
|  | **17-31 July 2017** | **Unit1:** Number System, Binary Arithmetic Operations.  | Multiple Choice Question Test |
|  | **01-31 Aug 2017** | **Unit1:**1’s and 2’s complement representation and its arithmetic. Binary codes and its types.**Unit2:** Logic gates. | Group discussion on binary codes |
|  | **01-30 Sept 2017** | **Unit2:** Boolean Algebra, Simplification using K-Map, Don’t care implementation of SOP & POS using NAND and NOR Gate.**Unit3:** Combinational Circuit Design Procedure, Mux, Demux, Decoder, Encoder, Code Converter. | Solved Problems on Boolean Algebra and K-Map |
|  | **01-31 Oct 2017** | **Unit3:** Parity Generator and checker, Binary adder, Binary Subtractor, Parallel Binary adder, 2’s complement binary adder/subtractor, binary multiplier, and digital comparator.**Unit4:** Introduction to sequential circuits and flip-flops. | Solved Problems on applications of combinational circuits. |
|  | **01-13 Nov 2017** | **Unit4:** Clocked (RS, JK, T, D, Master Slave JK), Excitation table of flip-flop, edge triggered flip-flop, Applications of flip-flops. | Group discussion  |

**Topics of Assignments/ Class Tests to be given to the Students:**

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| **Assignment 1** | Self complementing codes, parity bit, universal gates, De-Morgan’s law. |
| **Assignment 2** | Demultiplexer, code converter,2’s complement adder& subtractor |
| **Class Test** | **Test 1:** Number system and arithmetic’s.**Test 2:** Boolean algebra, SOP and POS forms, K-Map.**Test 3:** Combinational circuits.**Test 4:** Flip-flops. |