**Name of the Teacher:** Mandeep Kaur **Class:** B.Sc (Hons)-IT-I-SEM-V

**Subject:** Computer System Architecture  **Paper:** BSIT-501

**Lesson Plan**

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| **S No** | **Period** | **Topics to be Covered** | **Academic Activity to be Organized** |
|  | **17-31 July 2017** | **Basic Computer Organisation and Design:** Instruction Codes, Computer registers,Computer Instructions, Timing and Control, Instruction Cycle | Group Discussion and Flowcharts implementation of Instruction Cycle |
|  | **01-31 Aug 2017** | Memory reference instructions, Input-Output and Interrupt, Design of Basic computer, Design ofaccumulator logic**Central Processing Unit:** General registers Organization, Stack Organization, Instruction formats, Addressing Modes, Data Transfer and Manipulation, Program Control | Power Point Presentation, Solved Numerical Problems on Addressing modes.Multiple Choice Question Test  |
|  | **01-30 Sept 2017** | Program Interrupt, Reduced Instruction Set Computer (RISC), CISC characteristics.**Register Transfer and Microoperations:** Register Transfer Language (RTL), register transfer, Bus and Memory Transfers,  | Discussion on Application of CISC Architecture: Overlapped WindowsPower Point Presentation  |
|  | **01-31 Oct 2017** | Arithmetic Microoperations, Logic Microoperations, Shift Microoperations, Arithmetic Logic Shift Unit**Microprogrammed Control:** Control memory;  | Flowcharts implementation, Power Point Presentation and Quiz |
|  | **01-13 Nov 2017** | Address sequencing, microprogramsequencer, Design of Control Unit | Power Point Presentation |

**Topics of Assignments/ Class Tests to be given to the Students:**

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| **Assignment 1** | Design of Basic computer and accumulator logic |
| **Assignment 2** | Discuss Addressing Modes |
| **Class Test** | Instruction Codes, Computer registers, Computer Instructions, Timing and Control, Instruction Cycle, Memory reference instructions, Input-Output and Interrupt |