**Name of the Teacher:** Ms. Alpa Sharma  **Class:** BCA Sem-I

**Subject:** Logical Organization of Computers-I

**Lesson Plan**

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| **S No** | **Period** | **Topics to be Covered** | **Academic Activity to be Organized** |
|  | **17-31 July 2017** | Information Representation: Number Systems, Binary Arithmetic, Fixed point and Floating-point representation of numbers, BCD Codes, Error detecting and correcting codes, Character Representation - ASCII, EBCDIC.  | **Group Discussion** |
|  | **01-31 Aug 2017** | Binary Logic: Boolean Algebra, Boolean Theorems, Boolean Functions and Truth Tables.Binary Logic: Boolean Algebra, Boolean Theorems, Boolean Functions and Truth Tables. Canonical and Standard forms of Boolean functions, Simplification of Boolean Functions, Venn Diagram,  | **On Board Presentations on different topics** |
|  | **01-30 Sept 2017** | Karnaugh Maps. Digital Logic: Basic Gates -AND, OR, NOT, Universal Gates - NAND, NOR, Other Gates –XOR, XNOR etc. implementations of digital circuits | **Group Discussion** |
|  | **01-31 Oct 2017** | Combinational Logic-Characteristics, Design Procedures, analysis procedures. Combinational Circuits: Half Adder, Full Adder, Half Subtractor, Full Subtractor | **On Board Presentations on different topics**  |
|  | **01-13 Nov 2017** | Encoders, Decoders, Multiplexers, Demultiplexers, Comparators, Code Converters. | **20 min written test on random topic given on previous day** |

**Topics of Assignments/ Class Tests to be given to the Students:**

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| **Assignment 1** | Basic Gates -AND, OR, NOT, Universal Gates - NAND, NOR, Other Gates –XOR, XNOR |
| **Assignment 2** | Combinational Circuits: Half Adder, Full Adder, Half Subtractor, Full Subtractor |
| **Class Test** | Combinational Logic-Characteristics, Design Procedures, analysis procedures. Combinational Circuits: Half Adder, Full Adder, Half Subtractor, Full Subtractor Encoders, Decoders, Multiplexers, Demultiplexers, Comparators, Code Converters. |